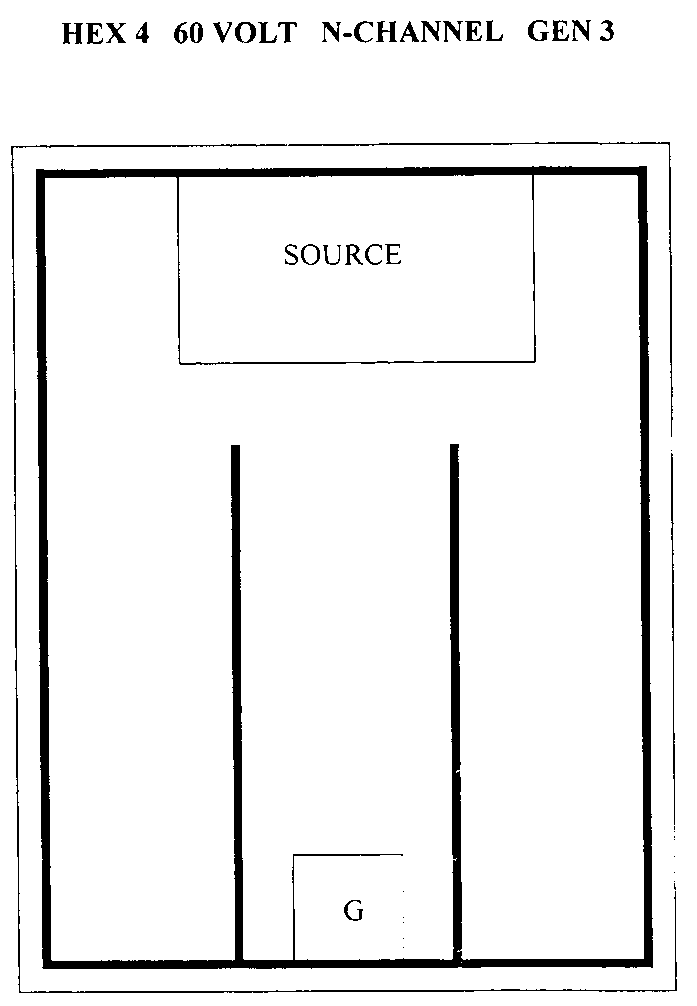
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .050” X .070” G = .020” X .022”**

**Backside Potential: Drain**

**Mask Ref: Gen 3**

**APPROVED BY: DK DIE SIZE .170” X .227” DATE: 8/30/21**

**MFG: IR THICKNESS .016” P/N: IRLC044B**

**DG 10.1.2**

#### Rev B, 7/19/02